REMARKS

This application has been reviewed in light of the Office Action mailed July 12, 2005. Reconsideration of this application in view of the below remarks, supplementing remarks made in the previous response dated October 12, 2005, is respectfully requested. Claims 1-13 are pending in the application with Claim 1 and 11 being in independent form. By the present amendment, Claims 1 and 3 have been amended and Claims 10-13 have been newly added. No new subject matter has been introduced by way of the present amendment.

Amended Claim 1 and newly added Claim 11 clearly point out the distinguishing features of the present invention. Specifically, the present invention utilizes the difference in current supply ability between a pair of transistors forming an inverter to reduce the physical size of this inventive inverter used in systems where only one of either the rising and falling edge of a reference clock is used, as well as reducing the size of an inverter driving the inventive inverter. Ultimately, a far reduced buffer size formed by the pair of such inverters is attained.

The prior art shown in Applicant's FIG. 7 (hereinafter referred to as "FIG. 7") uses transistors having the same current supply ability to form an inverter, thereby achieving a steep clock edge rise and fall. For a given gap width, P-channel and N-channel transistors have different current supply abilities because of the difference in carrier type. Therefore, in order to achieve the same current supply ability, the gate width of the P-channel and N-channel transistors needs to be different.

Amended Claim 1 recites: "...an inverter including: a first transistor of a first conductivity type for driving a load at one edge of the reference clock when said clock synchronous circuit does not operate in synchronization; and a second transistor of a second conductivity type for driving the load at the other edge of the reference clock when said clock

synchronous circuit operates in synchronization, the second transistor having a current supply ability larger than the first transistor." (Emphasis added).

Hence, the difference in the current supply ability between the first transistor and the second transistor is clearly claimed as a limitation of the present invention. The difference in the current supply ability between the two transistors of opposing carrier types can be determined by setting the current supply ability of any one of the two transistors. The setting is performed by operation of the synchronization circuit connected to the output terminal corresponding to either one of the rising and falling edges of the reference clock.

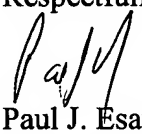
Accordingly, Applicant respectfully requests withdrawal of the rejection with respect to Claims 1-10 under 35 U.S.C. §102. Additionally, as Claim 11 recites similar limitations directed to a difference in current supply ability between two transistors, Claim 11, and the claims depending from Claim 11 are believed allowable over the prior art.

CONCLUSIONS

In view of the foregoing amendments and remarks, it is respectfully submitted that all claims presently pending in the application, namely, Claims 1-9 are believed to be in condition for allowance and patentably distinguishable over the art of record.

If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call Applicant's undersigned attorney at the number indicated below.

Respectfully submitted,



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